UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,620	08/07/2001	Marcus Tong	2001P4227US01	3155

7590 12/13/2005	EXAMINER
Siemens Corporation	CHANG, RICHARD
Attn: Elsa Keller, Legal Administrator	

ART UNIT	PAPER NUMBER
2663	

Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/924,620	TONG ET AL.
	Examiner	**Art Unit**	
	Richard Chang	2663	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>19 September 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-10, 12, 14, 16-20</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-10,12,14 and 16-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>07 August 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendments, filed on 09/19/2005, with respect to claims 1-10, 12,

14, and 16-20 have been fully considered but are moot in view of the new ground(s) of

rejection.

2. The indicated allowability of claim 1-10 and 19-20 are withdrawn in view of the

previously cited references to US patent No. 5,327,391 ("Hirata") and US patent No.

6,049,565 ("Paradine et al."), upon further consideration, a new ground of rejection is

made as follow.

Claims 11, 13 and 15 had been canceled.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10, 12, 14, and 16-20 are rejected under 35 U.S.C. 103(a) as being

unpatentable over US patent US patent No. 6,049,565 ("Paradine et al.") in view of US

patent No. 5,327,391 ("Hirata").

Regarding claims 1, 5, 12, 14, and 19, Paradine et al. teach an audio

communication method and apparatus over network traffic (See Fig. 1) comprising of

an audio input (305),

an audio output (340),

interface circuitry comprising first and second jitter buffers (320 double buffer) operably coupling said audio input (305) to a voice encoder (via CODEC) and third and fourth jitter buffers (330 double buffer) operably coupling said audio output (340) to a voice decoder (via CODEC circuitry block),

wherein said first or second jitter buffers (320 double buffer for audio IN path) alternately fill at a first clock frequency (sampling clock via CODEC circuitry block) and empty at a second clock frequency (clock on DSP side for network interface) (see Col. 4, lines 27-50),

wherein alternation between said first and second jitter buffers occurs at said second clock frequency (8 ms CCITT G.711 format frame for network interface, See Col. 5, lines 55-65), and

wherein said third or fourth jitter buffers (330 double buffer for audio OUT path) alternately fill at said second clock frequency (clock for network interface) and empty at said first clock frequency (clock for network interface), wherein alternation between said third and fourth jitter buffers (330 double buffer) occurs at said second clock frequency (8 ms CCITT G.711 format frame for network interface, See Col. 5, lines 55-65).

Paradine et al. teaches substantially all the claimed invention but did not disclose expressly the detailed structure of the double buffers besides their functionality and application.

Hirata teaches that the rate adaptation and jitter smoothing method with the double buffer structure comprising of

providing first circuitry (21, 25-1 and 25-2) in a first clock (101) domain operable

at a first clock (101) frequency,

providing second circuitry (22, 26-1 and 26-2) in a second clock (103) domain

operable at a second clock (103) frequency,

providing first and second jitter buffers (24-1 and 24-2) interfacing between said

first circuitry (11) and said second circuitry (12) domain,

wherein said first or second jitter buffers (24-1 and 24-2) alternately fill at said

first clock (101) frequency and empty at said second clock (103) frequency,

wherein alternation between said first and second jitter buffers (24-1 and 24-2)

occurs at said second clocking frequency (104) (See Fig. 1, Col 4, lines 4-49).

A person of ordinary skill in the art would have been motivated to employ Hirata

in Paradine et al. in order to obtain a method to manage double buffers across two

different clock domains for transmission of voice over network and to take advantage of

utilizing double buffers across different clock domains in claims *1, 5, 12, 14, and 19*.

The suggestion/motivation to do so would have been to utilize double buffers

across different clock domains, as suggested by Hirata in Col 4, lines 4-49. At the time

the invention was made, therefore, it would have been obvious to one of ordinary skill in

the art to which the invention pertains to combine Hirata with the Paradine et al. to

obtain the inventions specified in claims *1, 5, 12, 14, and 19*.

Regarding claims 2 and 16, these claims have similar limitation as claim 1 and

Paradine et al. further teach that said first circuitry comprising an audio input (305

microphone), said second circuitry comprising an encoder (315 DSP1) (See Fig. 7),

thus it is rejected with the same rationale applied against claim 1 above.

Regarding claims 3 and 17, these claims have similar limitation as claim 1 and

Paradine et al. further teach that said first circuitry comprising an audio input (340

speaker), said second circuitry comprising an decoder (315 DSP2) (See Fig. 7), thus it

is rejected with the same rationale applied against claim 1 above.

Regarding claim 6, these claims have similar limitation as claim 1 and Paradine

et al. further teach that said interface circuitry comprising one or more digital signal

processors (DSP) (See Col. 4, lines 43-50), thus it is rejected with the same rationale

applied against claim 1 above.

Regarding claims 4, 7-8 and 18, these claims have similar limitation as claims 1,

6 and 17 and Paradine et al. further teach that said first clock frequency comprising a

PCM sample clock (see Col. 4, lines 27-50), and said second clock frequency

comprising an 8 ms frame clock (See Col. 5, lines 55-65), thus it is rejected with the

same rationale applied against claims 1, 6 and 17 above.

Regarding claims 9-10, these claims have similar limitation as claim 8 and

Paradine et al. further teach that that the encoded voice data may be 8 ms frame based

such as 8 ms frame (See Col. 5, lines 55-65), it is obvious for 20 ms frame as 160

samples frame plus buffering for overflow as 165 samples per frame (See Col. 6, lines

46-50), thus it is rejected with the same rationale applied against claim 8 above.

Regarding claim 20, this claim has similar limitation as claim 19 and Paradine et

al. further teach that the encoded voice data may be transmitted based on CCITT G.711

format as 8 ms frame per voice data block, this is applicable to different frame sizes

voice codec such as GSM phone (See col. 6, lines 56-65), thus it is rejected with the

same rationale applied against claim 19 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Richard Chang whose telephone number is (571) 272-

3129. The examiner can normally be reached on Monday - Friday from 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

rkc

Richard Chang
Patent Examiner
Art Unit 2663

DERRICK FERRIS
PATENT EXAMINER